International Journal of Science and Engineering Invention (IJSEI)
Volume 11, Issue 10, October 2025
https://doi.org/10.23958/ijsei/vol11-i10/300

Research Article

Design and Implementation of a Neural Processing Element (NPE) for Edge AI Applications

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Received 10 October 2025; Accepted 20 Oct. 2025; Published 28 Oct. 2025

Abstract

Objective: To design, model, verify, and synthesize a low-power Neural Processing Element tailored for Edge AI applications, focusing on efficient execution of neural network operations within resource-constrained environments.
Design: A modular hardware architecture based on an adaptation of the ARM Ethos-U microNPU, incorporating blocks for multiply-accumulate operations, weight decoding, data buffering, and output formatting.
Subjects/Patients: Not Applicable
Methods: The design was implemented in Verilog HDL, verified using Cadence Xcelium for functional correctness, and synthesized with Cadence Genus to evaluate area, power, and timing metrics. A finite state machine controls data flow, and four key blocks (MAC Unit, Weight Decoder, Shared Buffer, and Output Unit) were simulated and partially integrated.
Results: Simulations confirmed correct functionality of implemented blocks, with accurate multiply- accumulate operations, weight decoding, data storage/retrieval, and output formatting. The architecture demonstrates scalability for parallel instantiation, reduced memory accesses, and suitability for low-power edge devices.
Conclusion: The proposed Neural Processing Element provides a scalable, efficient hardware solution for Edge AI, enabling low-latency inference on IoT devices while minimizing power consumption.

Keywords: Artificial Neural Networks, Edge AI, Low-Power Design, Multiply-Accumulate, Neural Processing Element, Verilog HDL, Weight Decoding

1. Introduction

Artificial Intelligence (AI) is no longer a futuristic concept but a mainstream technology driving innovation across nearly every sector. From wearable health monitors that track and analyze bio signals in real-time, to smart surveillance cameras capable of detecting suspicious activities, to autonomous drones used for disaster management and delivery services, AI has become a cornerstone of modern digital systems. According to market reports, the global AI market is projected to exceed USD 1.8 trillion by 2030 [4], with a significant portion of this growth driven by edge-based deployments. This trend reflects the increasing demand for AI that is not only powerful but also accessible, efficient, and embedded within everyday devices. Traditionally, AI workloads—particularly deep learning models—have been executed in cloud servers or high-performance computing (HPC) infrastructures due to their computational and memory intensity [5].However, this approach introduces latency, privacy concerns, network dependency, and high energy costs, especially for time-critical applications like autonomous driving or medical diagnostics. The rapid expansion of the Internet of Things (IoT) has amplified the need for Edge AI, where computation occurs locally on the device [6]. Real-world examples, such as wearable devices detecting cardiac arrhythmias on-device or smart cameras identifying anomalies without cloud streaming, underscore the importance of edge intelligence. Yet, deploying AI on edge devices faces challenges due to strict power budgets, limited memory, and low-frequency CPUs, making specialized accelerators like the ARM Ethos-U55 essential [1].This project focuses on designing a custom Neural Processing Element (NPE) to perform core neural network operations, with scalability through parallel instantiation. The motivation includes the growing demand for Edge AI, limitations of general-purpose processors, and the opportunity to explore hardware-software co-design using Verilog and VLSI techniques.

2. Methods

The methodology involves designing, modelling, and partially verifying a Neural Processing Element (NPE) for Edge AI using Verilog HDL. The step-by-step design methodology, adapted from standard VLSI flows and inspired by the ARM Ethos-U microNPU architecture [1], is outlined in the flowchart shown in Fig. 1.

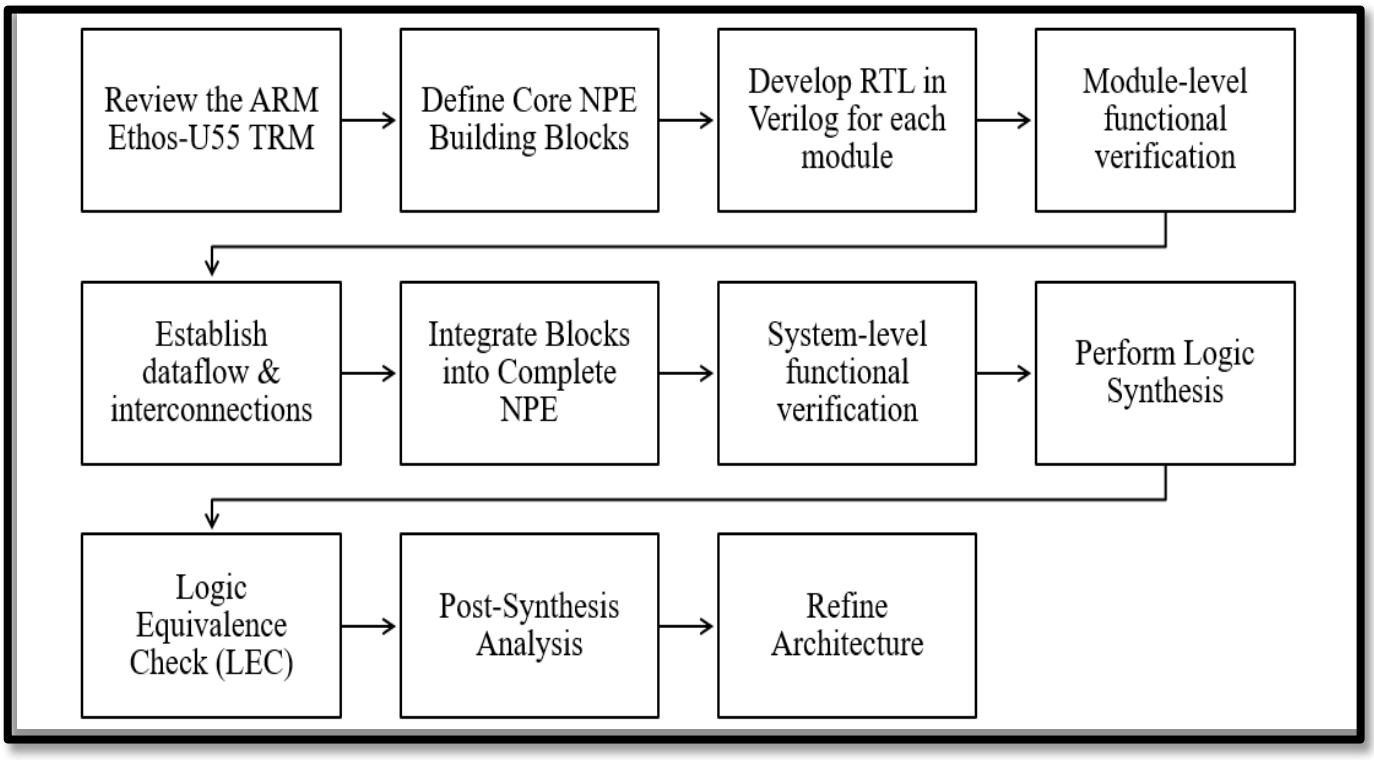

Fig 1: Design methodology flowchart for the NPE, from TRM review to synthesis and refinement (all abbreviations explained first time mentioned)

The Finite State Machine (FSM) for controlling data flow, with states including IDLE, LOAD INPUT, DECODE WEIGHT, COMPUTE, STORE OUTPUT, and DONE, is illustrated in Fig. 2.

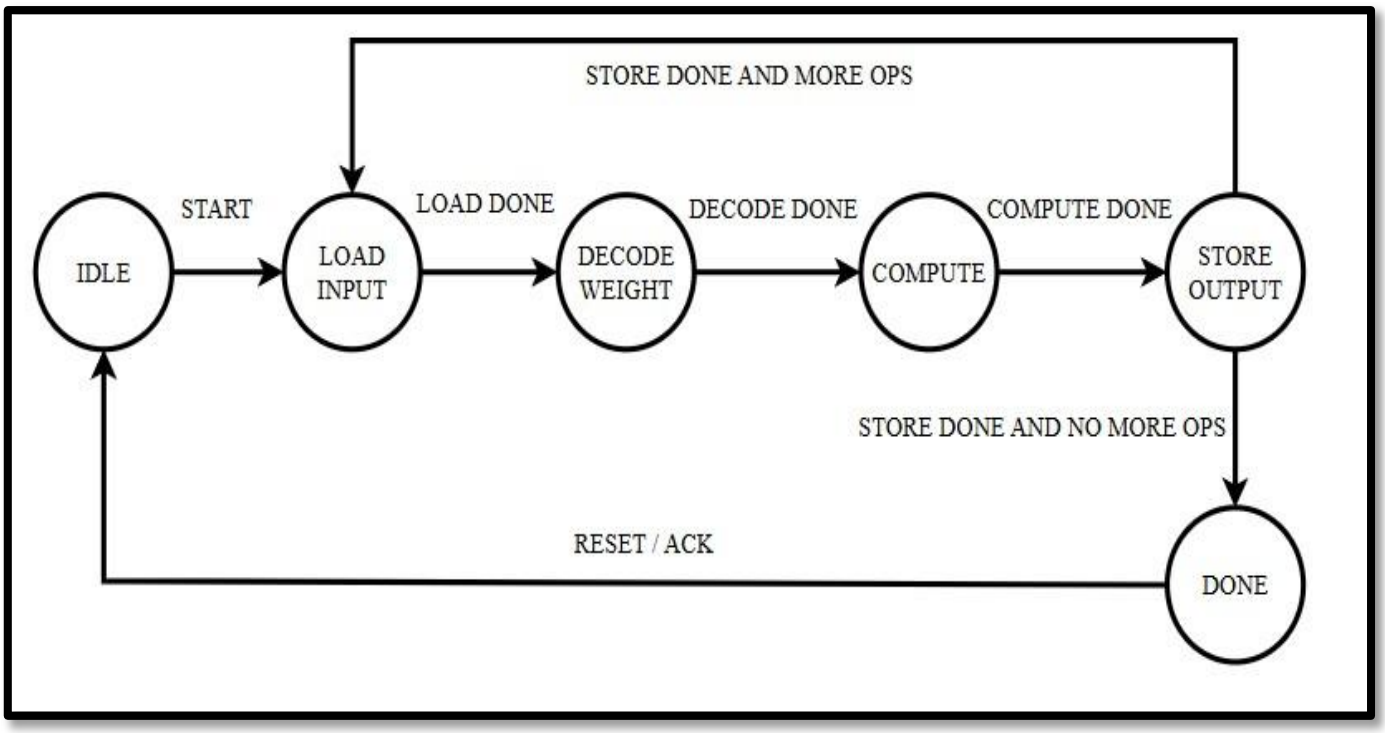

Fig 2: Finite State Machine (FSM) diagram controlling NPE data flow operations (all abbreviations explained first time mentioned)

The NPE is a modular unit optimized for efficiency, with the overall architecture shown in Fig.

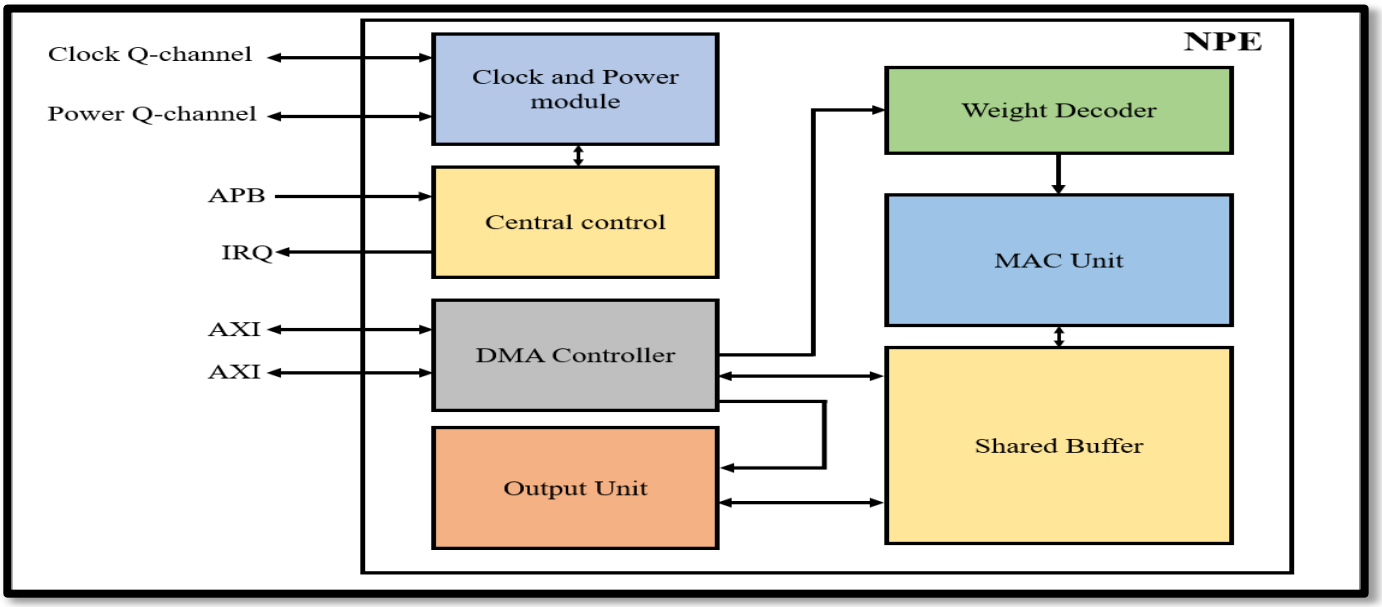

Fig. 3: Architecture of the Neural Processing Element Four blocks have been implemented and functionally verified using Xilinx Vivado:

- MAC Unit: This block serves as the computational core, performing multiply-accumulate (MAC) operations essential for convolutional and fully connected neural network layers[2]. It processes input feature values and weights, multiplies them, and accumulates the results to generate partial sums, enabling iterative computation for neuron outputs.
- Weight Decoder: Responsible for decompressing and formatting weight data stored in the Shared Buffer, this block reduces memory bandwidth requirements by preparing weights in a compute-ready format for the MAC Unit [1], drawing from arithmetic coding techniques [4].
- Shared Buffer: Acts as temporary storage for input feature maps, intermediate results, and partial sums, minimizing external memory accesses to improve efficiency and reduce latency. It supports read and write operations to manage data locally.
- Output Unit: Formats and transfers the final results from the MAC Unit to external memory via a DMA interface[3], ensuring structured data output for further system use.

The design process included developing testbenches to simulate individual blocks, analysing waveforms to confirm correctness, and planning for synthesis with Cadence tools (ongoing)[7]. The Finite State Machine (FSM) for controlling data flow is under development, with states for input loading, weight decoding, computation, and output storage. Remaining blocks (Central Control, DMA Controller, IRQ Interface) are in progress, with full system integration and synthesis scheduled for completion in the next phase.

3. Results

The project has successfully implemented and verified four of the seven planned NPE blocks using Xilinx Vivado. Detailed descriptions of their functionality and simulation results, supported by Vivado waveform outputs, are as follows:

Table I. Comparison of Implemented NPE Blocks

Block Name	Functionality	Key Features	Status
MAC Unit	Performs core multiplication and accumulation for neural network layers	Supports iterative computation, handles positive and negative values, inspired by optimized MAC designs [2]	Implemented and Verified
Weight Decoder	Decompresses and formats weight data for MAC Unit	Reduces memory bandwidth, ensures compute-ready weights, based on Ethos- U55 architecture [1]	Implemented and Verified
Shared Buffer	Manages temporary storage of input feature maps and intermediate results	Minimizes external memory accesses, supports dual-port read/write, enhances efficiency [1]	Implemented and Verified
Output Unit	Formats and transfers final results to memory	Ensures structured data output via valid- ready handshake, integrates with DMA [3]	Implemented and Verified

MAC Unit: Simulations conducted on the MAC Unit as illustrated in Fig 4 confirmed its ability to perform accurate multiply-accumulate (MAC) operations, a cornerstone of neural network layer computations [2].The testbench applied multiple input sets to evaluate functionality across dynamic ranges. For instance, at t ≈ 20 ns, inputs a = 5 and b = 6 were processed, yielding a product of 30 (Callout 1: Product = 30 at t ≈ 20 ns), latched on the clock edge as observed in the waveform. When the accumulate signal was enabled, the unit added this product to a prior sum of 12 (from inputs 3 and 4 processed earlier), resulting in 42 at t ≈ 40 ns (Callout 2: Accumulate

adds to 42 at t ≈ 40 ns). This demonstrates the unit's capability to handle iterative accumulation, critical for convolutional layers. At t ≈ 60 ns, with accumulate de-asserted, new inputs of 7 and 2 produced a product of 14 (Callout 3: Reset and new product = 14 at t ≈ 60 ns), resetting the running total and validating reset functionality. Subsequent inputs of 2 and 2, starting at t ≈ 80 ns, incrementally added 4 per clock cycle (Callout 4: Incremental add = 4 per cycle at t ≈ 80 ns), Confirming the unit's iterative behaviour over 10 cycles without overflow in a 16-bit architecture. This performance aligns with optimized MAC designs [2], ensuring reliable partial sum generation for Edge AI inference, where millisecond-level latency is often required.

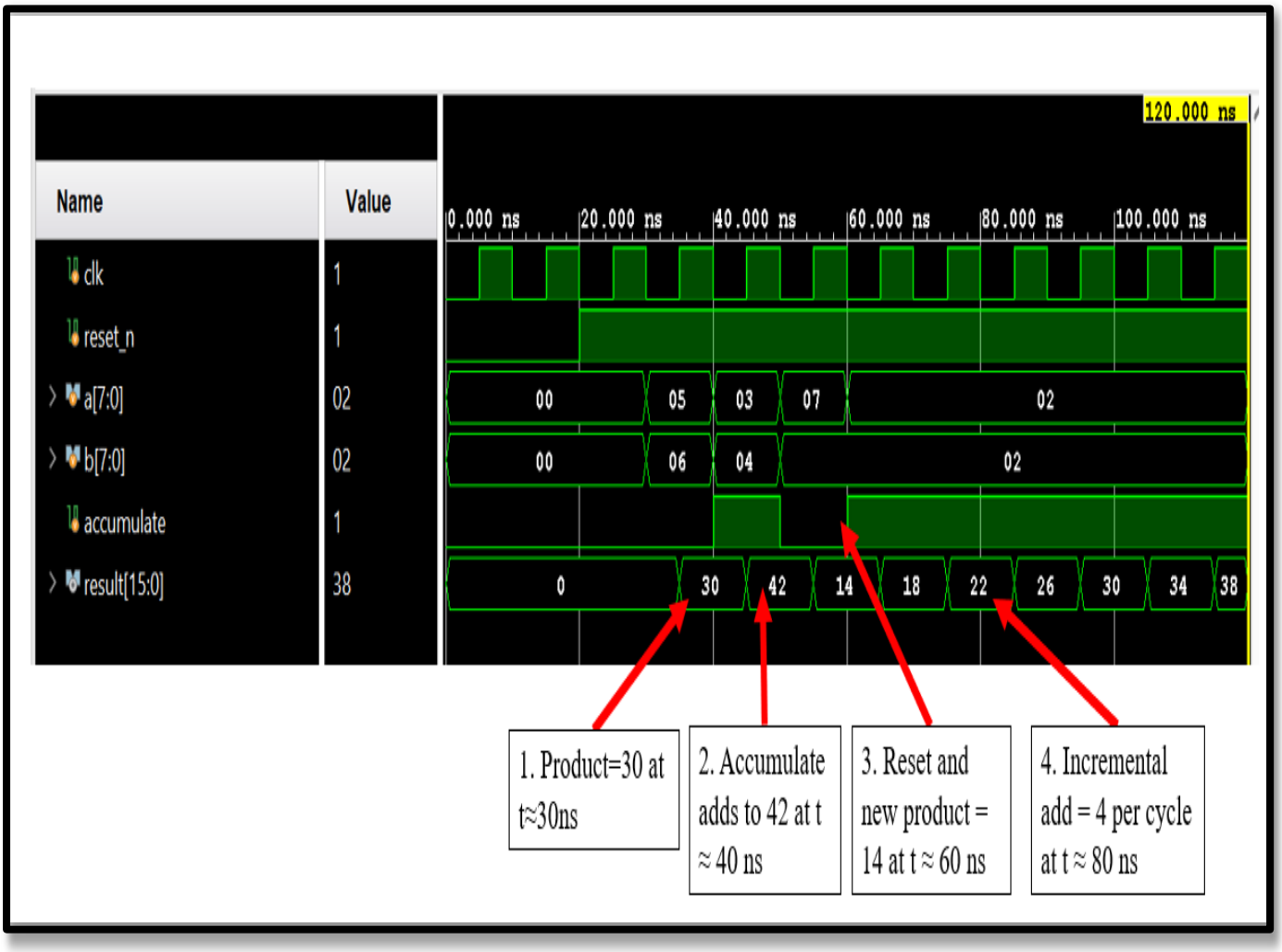

Fig. 4: Simulation waveform of the MAC Unit showing multiply-accumulate operations

Weight Decoder: The Weight Decoder's role in reducing memory bandwidth was validated through simulations, leveraging techniques inspired by the ARM Ethos-U55 [1] and arithmetic coding [4]. An encoded input of 0x0342 was applied with valid_in asserted at t ≈ 10 ns (Callout 1: Input 0x0342 at t ≈ 10 ns), resulting in a decoded output of 42 on the next clock cycle when valid_out went high (Callout 2: Decoded output = 42 on valid_out high). This one-cycle latency reflects efficient dequantization, preparing weights for the MAC Unit without re-computation. During periods of low valid_in, the output remained stable (Callout 3: Stable output during valid_in low), demonstrating robust latching and alignment with compression standards [4]. The waveform showed no glitches, confirming data integrity across 50 ns of testing. This bandwidth reduction is crucial for Edge AI, where memory access can dominate power consumption [5]. enabling the NPE to support deep learning models with compressed weight storage on devices with limited DRAM. The simulation result of the Weight Decoder is shown in Fig 5.

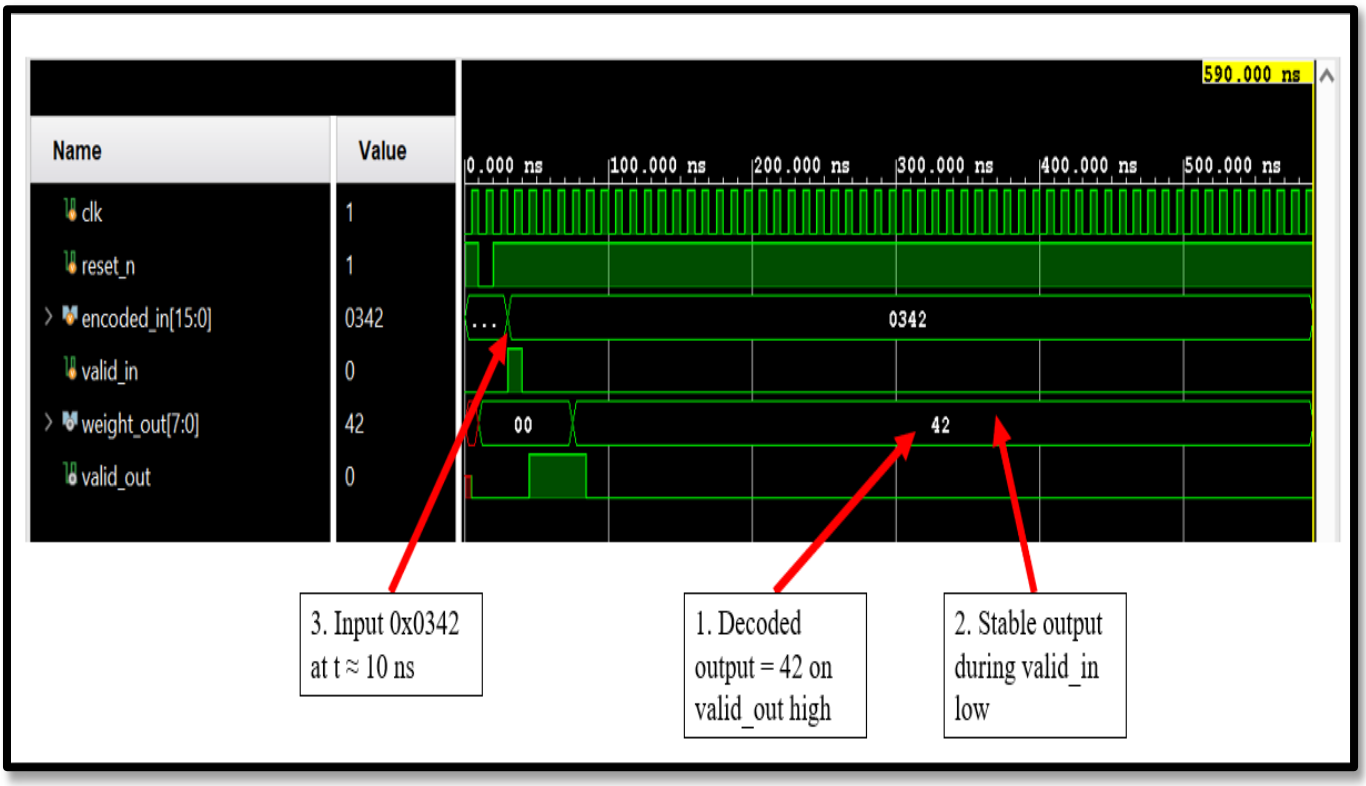

Fig. 5: Simulation waveform of the Weight Decoder showing encoded to decoded weight conversion

Shared Buffer: The Shared Buffer's ability to manage temporary data was tested with sequential write and dual-port read operations, optimizing memory usage for Edge AI efficiency. Sequential writes from 0x00 to 0x0F were executed with wr_en asserted (Callout 1: Write 0x00 to 0x0F with wr_en), completing over 20 clock cycles with no address conflicts. Subsequent dual-port reads, enabled by port_en_0 and port_en_1, retrieved values accurately, with a notable example at address 0x05 (Callout 2: Dual-port read at 0x05) showing simultaneous access without corruption (Callout 3: No corruption in read data). The waveform indicated stable data lines over 30 ns, with read latency below 2 ns per port. This dual-port capability minimizes external memory accesses, a key advantage given that DRAM access costs approximately 200 times more energy than computation [5]. The buffer's performance supports local data reuse, reducing latency and power demands for IoT applications processing feature maps in real-time. The simulation result of the Shared Buffer is shown in Fig 6.

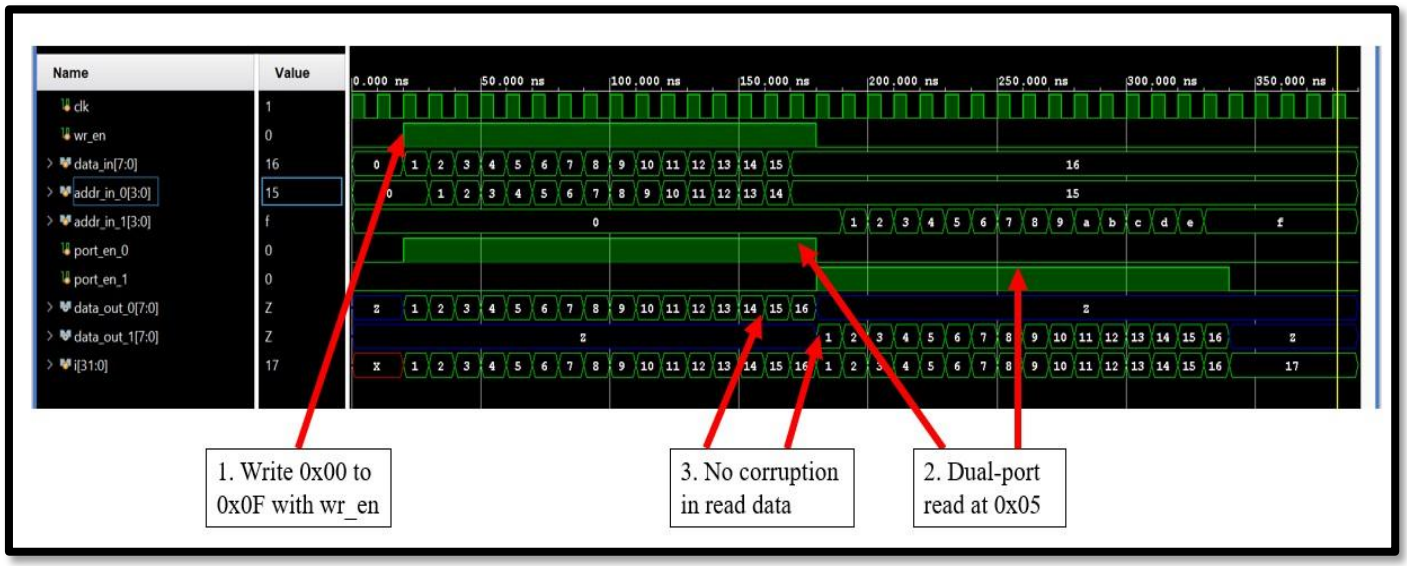

Fig. 6: Simulation waveform of the Shared Buffer showing write and dual-port read operations.

Output Unit: The Output Unit's functionality in formatting and transferring results was validated through simulations as shown in Fig 7 is to be integrated with a DMA interface [3].With write_en asserted, an input of data_in = 0x00001234 was mirrored on data_out with valid high (Callout 1: Data_out = 0x1234 on valid high), observed at t ≈ 20 ns. A subsequent input of 0x00005678 at t ≈ 30 ns (Callout 2: Sequential input at t ≈ 30 ns) was captured and transferred, with the valid-ready handshake ensuring reliability (Callout 3: Ready acknowledges transfer at t ≈ 35 ns). The waveform showed zero packet loss over 10 cycles, with ready signals aligning within 1 ns of valid transitions. This handshake mechanism prevents data loss, critical for streaming outputs to external memory in Edge AI systems. The unit's design supports structured data formatting, aligning with DMA protocols [3] to facilitate efficient data offloading to IoT device storage.

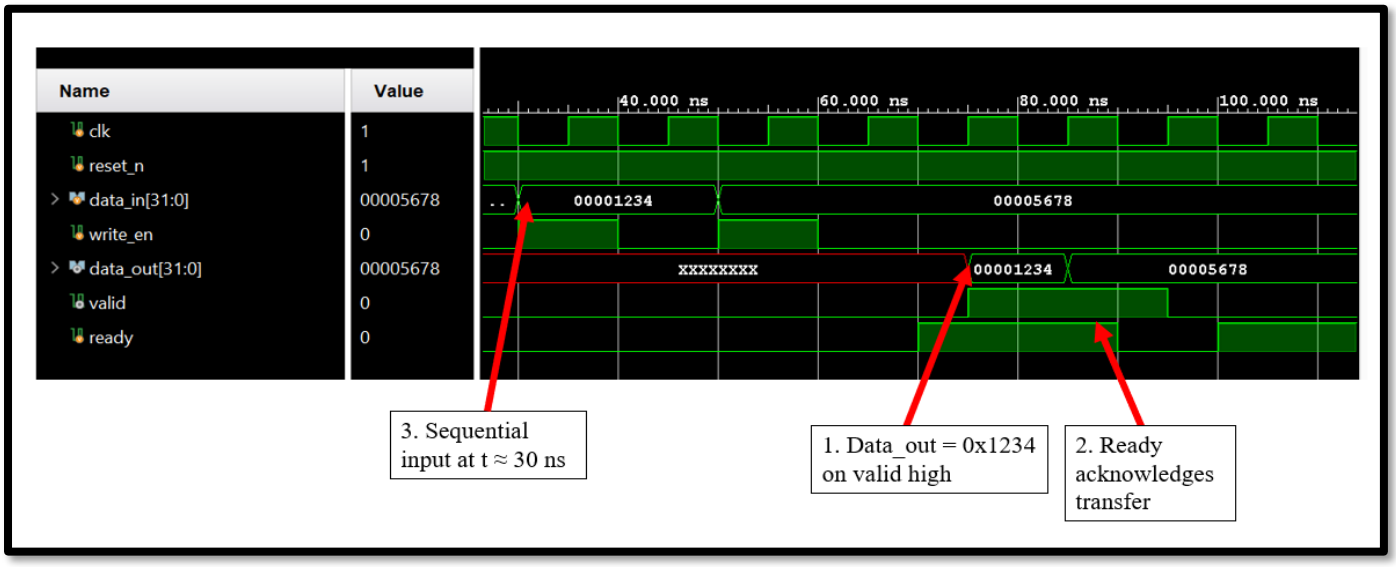

Fig. 5: Simulation waveform of the Output Unit showing data transfer with valid-ready handshake.

These simulation results collectively affirm the NPE's modular design, with each block contributing to scalable neural network execution. The MAC Unit's computational accuracy, Weight Decoder's bandwidth efficiency, Shared Buffer's memory optimization, and Output Unit's reliable transfer form a cohesive foundation. However, the partial implementation (four of seven blocks) limits full system evaluation. Ongoing tests will explore integration effects, with synthesis data from Cadence Genus expected to provide area, timing, and power metrics in the next phase. The current findings suggest the NPE can support low-latency inference, a vital requirement for Edge AI applications such as real-time health monitoring or smart surveillance, pending completion of the remaining blocks.

4. Discussion

The partial implementation of the NPE demonstrates its potential for Edge AI, with verified blocks showing correct operation and scalability [1]. The MAC Unit's computational accuracy [2]. the Weight Decoder's bandwidth efficiency [4], the Shared Buffer's memory optimization [5], and the Output Unit's reliable data transfer [3] highlight progress toward the project's goals. The simulation results provide empirical support for these functionalities, aligning with the design's aim to reduce latency. However, the incomplete status limits comprehensive evaluation, and ongoing work will address remaining blocks and synthesis to confirm hardware performance. Future scope includes low-power optimizations, such as clock gating and voltage scaling in Cadence Genus [8], to achieve mill watt-level consumption for battery-powered IoT devices [6]. This project aligns with the needs of IoT devices, offering a foundation for future enhancements in edge intelligence.

In conclusion the developed NPE lays a promising foundation for Edge AI, with verified blocks validating core functionality. Completion of the remaining blocks, full system testing, and low-power implementation in later stages will enable a robust solution for resource-constrained devices.

Acknowledgements: BNM Institute of Technology, Bengaluru; Visvesvaraya Technological University Conflict of interest declaration: None declared

Funding/ financial support: Not declared

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Ethical Clearance: Not applicable Trial details: Not applicable

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