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Research Article

Low Power-Aware ATPG for Scan Based Testing

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Abstract

The relentless scaling of semiconductor technology, leading to higher gate densities and lower operating voltages, has introduced a critical bottleneck in manufacturing: excessive power dissipation during scan-based testing. While essential for achieving high fault coverage, conventional Automatic Test Pattern Generation (ATPG) methodologies are power-agnostic. Their primary objective is maximizing fault coverage, often resulting in test patterns that induce unrealistic switching activity, which can cause thermal hotspots, severe IR drop, and ultimately reduce device reliability. These power violations can lead to immediate yield loss or latent, in-field failures. This paper details a comprehensive power-aware ATPG methodology designed to mitigate these risks without compromising test quality. The proposed framework integrates two synergistic techniques: scan chain reordering, which structurally minimizes shift transitions by optimizing the physical order of flip-flops based on their proximity, and intelligent X-filling, which strategically assigns logic values to "don't care" bits to actively prevent unnecessary switching. This approach transforms previously random don't-care bits into a powerful tool for power reduction. The methodology was implemented and validated on a T80 processor core synthesized using a 90nm technology node. Results were benchmarked against a conventional ATPG flow, demonstrating a dramatic reduction in average shift switching activity, which was consistently constrained below 25% compared to erratic peaks over 50% in the baseline. Furthermore, peak capture power remained well within the design's switching budget. This work validates a practical and scalable solution that directly contributes to enhanced manufacturing yield, improved chip reliability, and reduced test costs, making it a fundamental requirement for producing complex modern SoCs.

Keywords: ATPG, Design-for-Testability (DFT), Low-Power Testing, Scan-Based Testing, Switching Activity, IR Drop, X-Filling.

1. Introduction

Modern Systems-on-Chip (SoCs) now integrate billions of transistors, powering everything from mobile devices to safety-critical automotive systems. This immense complexity makes rigorous post-manufacturing testing an indispensable phase of production to screen for physical defects that are inherent to the semiconductor fabrication process. Scan-based testing has become the industry-standard Design-for-Testability (DFT) technique, providing the necessary controllability and observability to achieve high fault coverage. This is achieved by stitching the design's flip-flops into long scan chains, effectively transforming a complex sequential circuit into a simple shift register during test mode, which provides unparalleled access to internal circuit nodes.

However, this ubiquitous method harbors a significant drawback. The process of shifting long test patterns through scan chains induces massive, uncorrelated switching activity—often causing 50% or more of a chip's flip-flops to toggle simultaneously. This behavior is fundamentally different from in-field operation, where switching is typically localized and functionally correlated. This power surge, which can be several times higher than the worst-case functional power, creates a dangerous disconnect between design intent and test reality. The consequences are severe: thermal hotspots that risk permanent damage, power integrity failure (IR drop) leading to costly false failures by causing setup and hold time violations on perfectly good circuits, and accelerated aging that compromises long-term reliability through mechanisms such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI).

Conventional ATPG tools, optimized solely for fault coverage and pattern count, are fundamentally "power-blind" and fail to address this challenge. They operate at a high level of abstraction, treating the silicon as an ideal switching fabric while ignoring the physical constraints of the power delivery network (PDN). This paper enters this pragmatic space, arguing that test power must be treated as a first-class design constraint, not an afterthought. By developing and validating an integrated power-aware ATPG methodology, this work aims to bridge the gap between test quality and test safety, offering a robust framework for generating test patterns that are both highly effective at detecting defects and certifiably safe for the device under test.

2. Literature review

The challenge of excessive power dissipation during scan-based testing has been a persistent concern in VLSI design for decades. As technology nodes shrink and System-on-a-Chip (SoC) complexity grows, the power consumed during test can far exceed that of functional operation, leading to thermal damage, IR drop-induced false failures, and long-term reliability degradation.

The academic literature has extensively addressed this issue, evolving from foundational techniques targeting specific aspects of the problem to comprehensive, integrated solutions. Early research recognized the root of the problem in the high, uncorrelated switching activity induced by test patterns. Pioneering work by Wang and Gupta (1997) [6] established the need for modifying the Automatic Test Pattern Generation (ATPG) process itself to minimize heat dissipation.

This vector-centric approach was refined through techniques focused on "don't care" (X-bit) filling, with research by Rosinger et al. (2002) [9] providing methods for assessing switching activity to enable more intelligent algorithms. The concern also extended to Built-in Self-Test (BIST), where techniques like test vector inhibiting were proposed [5, 10]. Concurrently, another school of thought focused not on the test patterns, but on the underlying Design-for-Testability (DFT) structure. Seminal papers by Jas et al. (2003) [3] and Sankaralingam et al. (2002) [4] introduced powerful structural techniques like scan chain reordering and scan gating.

This research remains highly active, with recent studies by Annamareddy & Mohan (2024) [1] and Reddy & Reddy (2022) [2] proposing improved scan chain stitching algorithms that consider modern constraints like logic topology and routing. As the field matured, researchers began to develop more holistic solutions that integrated multiple techniques.

A natural synergy was found between test data compression and power reduction, as explored by Chandra & Chakrabarty (2004) [11] and Larsson & Saluja (2007) [12]. The scope also expanded to the entire SoC with power-aware test scheduling [14], acknowledging that test power is a global chip-level constraint [15]. Recent comprehensive methodologies from Abdel-Hafez et al. (2022) [7] and Zhong & Guin (2024) [8] exemplify the modern approach, creating unified frameworks to manage the power demands of testing today's complex SoCs.

3. Methodology

The project methodology follows an industry-standard VLSI design and test flow, executed using a suite of Cadence EDA tools. The process begins with the specification and synthesis of the Design Under Test (DUT), proceeds through comprehensive Design-for-Testability (DFT) insertion, and culminates in a detailed comparative analysis between a standard, coverage-focused Automatic Test Pattern Generation (ATPG) flow and a novel power-aware ATPG flow.

3.1 Design Specification and Synthesis

The circuit chosen as the DUT is the T80 processor core, an open-source Verilog model of a Z80-compatible microprocessor. This core was selected because its substantial complexity, featuring a rich mix of sequential and combinational logic elements as well as a defined control path and datapath, provides a realistic and challenging test case for investigating modern DFT and ATPG challenges. It is representative of a medium-sized intellectual property (IP) block commonly found in larger SoC designs.

The design process began with the synthesis of the high-level Register-Transfer Level (RTL) code. Synthesis is the automated process of translating the abstract behavioral description of the circuit (Verilog) into a physically realizable, gate-level netlist. This critical step was performed using the Cadence Genus Synthesis Solution, targeting a 90nm digital standard cell library (slow.lib). The choice of a 90nm node is representative of a mature technology still widely used in many applications. The entire synthesis process was governed by a Synopsys Design Constraints (SDC) file. This file is paramount, as it directs the synthesis tool to not only create a logically correct circuit but also one that can meet performance targets. It defined a primary clock frequency of 100 MHz, along with other essential I/O timing parameters, operating conditions, and wire load models to guide the tool in achieving timing closure.

3.2 DFT Scan Insertion

After a functionally correct and timing-clean gate-level netlist was generated, it was augmented with a muxed-scan DFT architecture. Scan insertion is the cornerstone of modern DFT, transforming a hard-to-test sequential circuit into a much simpler combinational one during test mode. This is achieved by replacing all standard flip-flops with scan cells. Each scan cell contains an additional multiplexer on its input, allowing it to source data either from the functional logic (for normal operation) or from the output of the previous scan cell in a chain (for test operation).

These scan cells were then stitched into a single, continuous scan chain, effectively creating a massive shift register that runs through the entire design. This architecture provides full controllability and observability of the circuit's internal states. Controllability refers to the ability to set every flip-flop to a desired logic value (0 or 1) by shifting a pattern in through the scan-in port. Observability refers to the ability to capture the circuit's response to that pattern and read out the state of every flip-flop through the scan-out port. This process was automated within Cadence Genus using a detailed Tool Command Language (TCL) script, which specified the scan chain configuration, defined the test-specific signals (like scan enable and the test clock), and executed the stitching process.

3.3 ATPG Flow and Power-Aware Techniques

With a test-ready netlist, the workflow bifurcates into two parallel paths for comparative analysis, as shown in Figure 1.

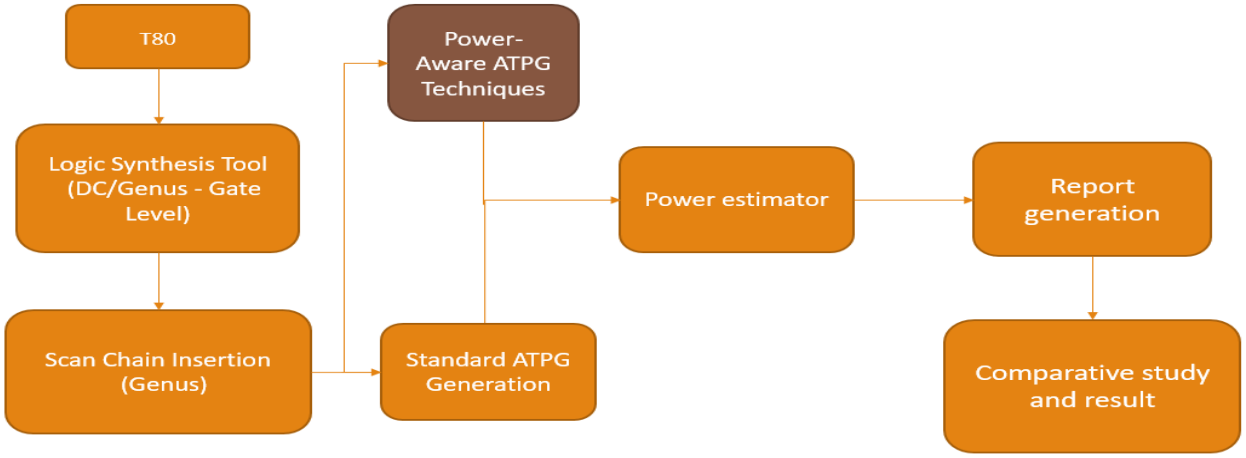

Figure 1: Design Flow for ATPG

Standard ATPG (Baseline): The first path generates a conventional set of test vectors using the Cadence Modus ATPG tool. This flow is optimized solely for achieving maximum stuck-at fault coverage and minimum pattern count, serving as the performance and power benchmark.

Standard ATPG (Baseline): The first path generates a conventional set of test vectors using the Cadence Modus ATPG tool. This flow is configured with traditional objectives: achieve the highest possible stuck-at fault coverage with the minimum number of test patterns. The stuck-at model, which assumes a circuit node is permanently fixed to logic 0 or 1, is the industry's primary metric for test quality. This baseline flow is deliberately "power-blind," meaning it does not consider the switching activity or power consumption of the patterns it generates. The resulting high-coverage, compact test set serves as the critical performance and power benchmark against which the experimental flow is measured.

Power-Aware ATPG (Experimental): The second path employs a suite of advanced low-power techniques within Modus to generate an optimized test set. This is a multi-faceted approach that attacks test power from both a vector-based and a structural perspective. Key techniques include:

Transition Weighting: The core ATPG algorithm is modified to assign a "cost" to signal transitions. During its search for a pattern to detect a specific fault, the algorithm explores a decision tree. This modification prunes branches that lead to high switching activity, preferentially selecting patterns with the lowest transition cost, thus generating inherently lower-power vectors.

X-Filling: "Don't care" (X) bits, which represent logic values not required for detecting a target fault, are intelligently filled. Instead of random assignment (which yields a 50% transition probability), methods like adjacent-fill are used. This heuristic fills an X-bit with the same value as its neighboring bit in the scan chain, actively preventing state changes during the scan shifting process.

Scan Chain Partitioning/Reordering: This structural technique leverages physical design information to reorder the scan cells. By placing physically proximate flip-flops next to each other in the scan chain, the technique exploits the fact that nearby logic often has correlated activity, naturally reducing random switching during shift and thus lowering overall power consumption.

The outputs from both paths—including test patterns, fault coverage reports, and detailed power analysis reports—are then used for a final comparative study to precisely quantify the effectiveness of the power-aware methodology in reducing test power without compromising test quality.

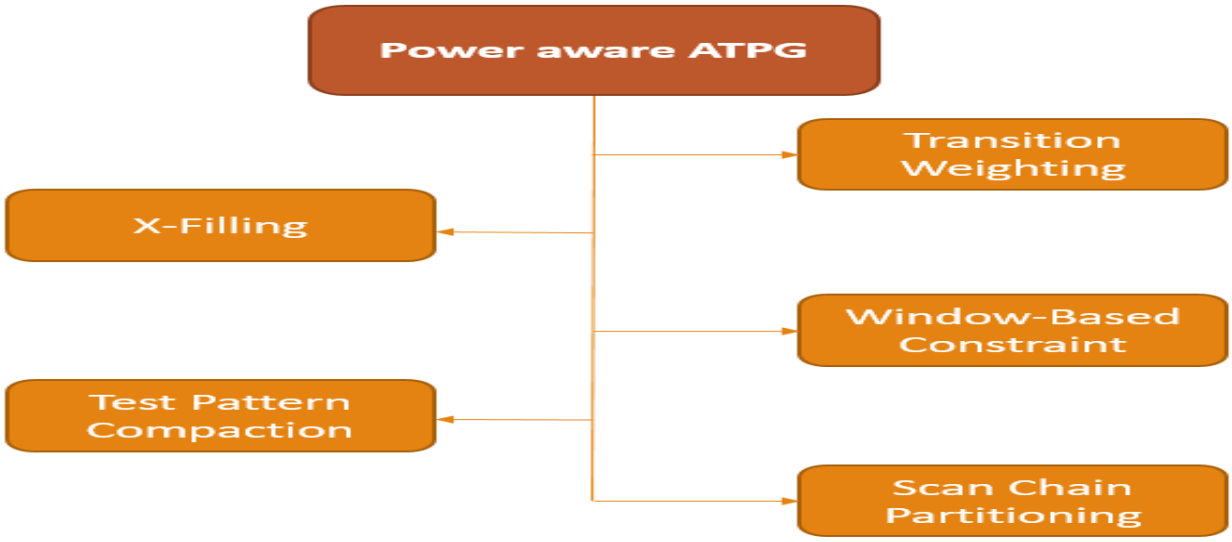

Figure 2: Power-Aware ATPG Techniques

The outputs from both paths, including test patterns and power reports, are then used for a final comparative study to quantify the effectiveness of the power-aware methodology.

4.0 Results and Discussion

The experimental implementation on the T80 processor core yielded clear, quantitative data demonstrating both the physical overhead of implementing DFT and the significant efficacy of the power-aware ATPG methodology. The following sections provide a detailed breakdown and interpretation of these findings.

4.1 Synthesis and DFT Overhead

The initial synthesis of the T80 core from its RTL description resulted in a compact, gate-level netlist comprising 165 standard cells and 183 nets. This represents the baseline physical footprint of the functional design. After the DFT scan insertion process was completed, these metrics increased to 208 standard cells and 225 nets. This equates to a 26% increase in cell count and a 23% increase in net count. This overhead is an expected and well-understood trade-off in DFT implementation, primarily attributed to the replacement of smaller, area-efficient standard flip-flops with larger, more complex scan cells. Each scan cell's integrated multiplexer adds to the silicon area and introduces new routing complexity.

Furthermore, the number of top-level ports on the DUT increased from 27 to 30. This was necessary to accommodate the dedicated test signals required to control the scan architecture: a scan_in port to load test patterns, a scan_out port to observe the results, and a scan_enable signal to switch the circuit between its functional and test modes. While this area overhead is a direct cost of testability, it is considered essential in modern design for guaranteeing manufacturing quality and enabling effective failure analysis.

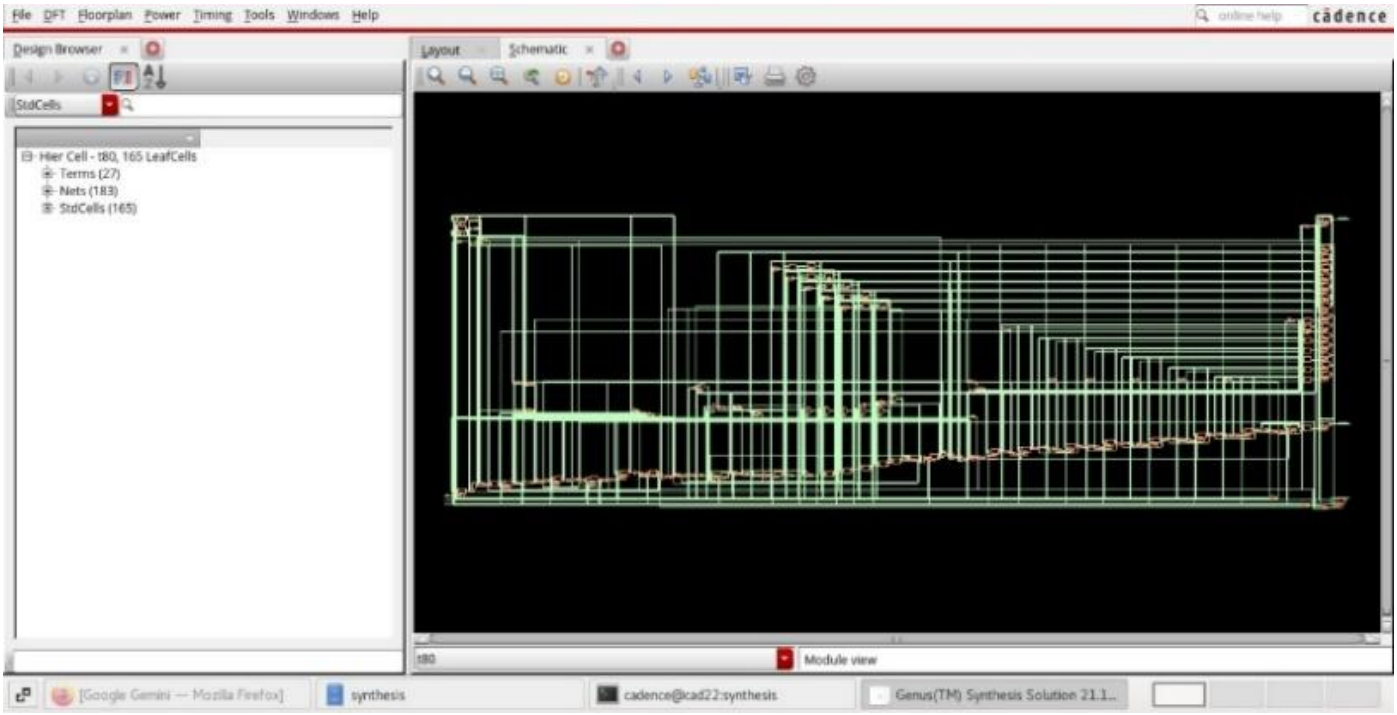

Figure 3: Synthesis of the T80 Circuit (Pre-DFT)

Figure 3 displays a gate-level view of the T80 processor core after synthesis, viewed within the Cadence Genus Synthesis Solution, an industry-standard EDA tool. The main window on the right shows the circuit's physical representation. The green boxes and lines are the standard cells (fundamental logic gates like AND, NAND, and flip-flops) and the nets (wires) that connect them. This is the result of translating the high-level Verilog code into a structural netlist using a 90nm technology library.

The "Design Browser" on the left provides a hierarchical summary, confirming the design is the "T80" and quantifying its size at 461 leaf Cells. Crucially, this view is labeled "Pre-DFT" (Design-for-Testability).

This means you are seeing the purely functional design, optimized for its operational purpose. It has not yet been modified to include the special scan-cell logic necessary for efficient manufacturing testing. The subsequent step in the design flow would be to insert these test structures, which would increase the cell count and prepare the chip for pattern generation.

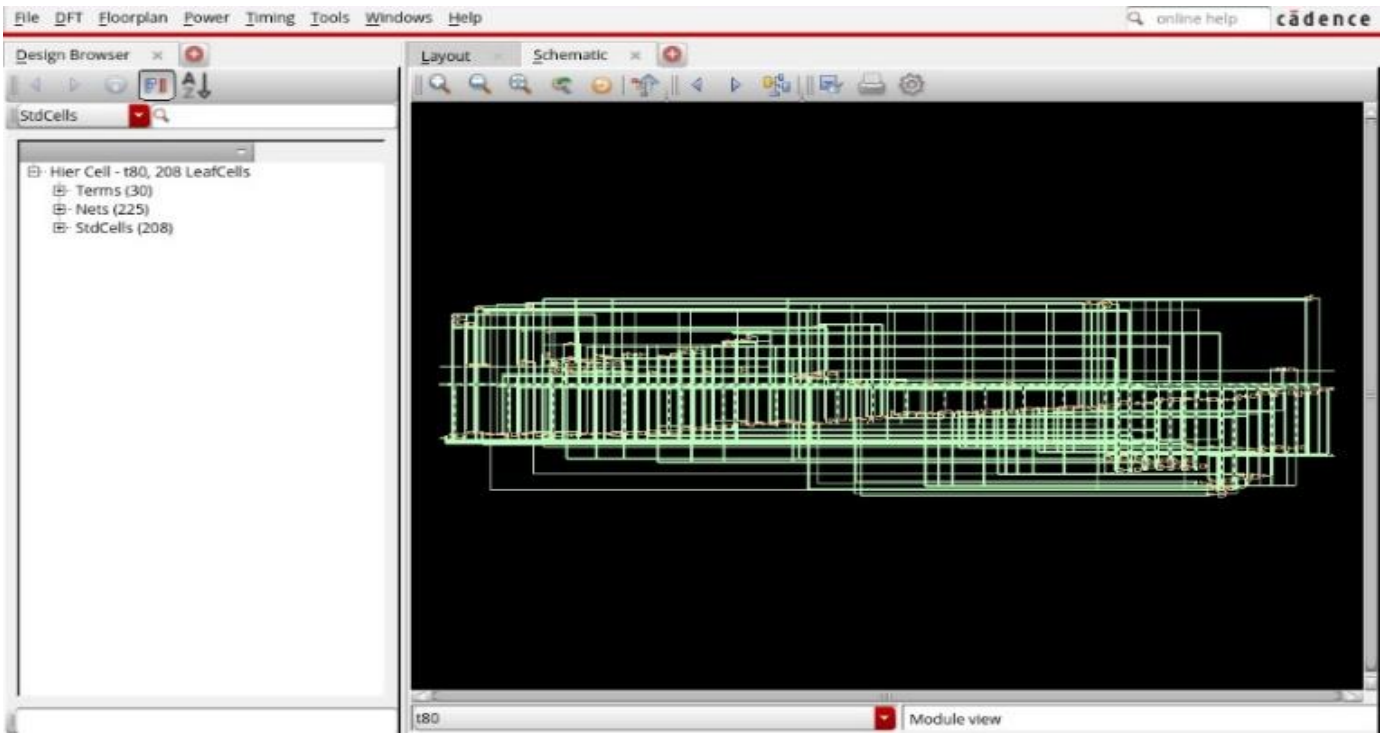

Figure 4: Synthesis after Scan Insertion (Post-DFT)

Figure 4 shows the T80 processor core after the crucial "Post-DFT" (Design-for-Testability) stage. The circuit has been modified to ensure it is fully testable for manufacturing defects. This was achieved by automatically replacing the original flip-flops with specialized scan cells and then "stitching" them together to form a continuous scan chain. This chain acts like a shift register, providing direct access to the chip's internal states for testing. The most significant result of this process is the increase in design size, a necessary trade-off for testability. The Design Browser on the left confirms this, now reporting 208 LeafCells. This increase is because scan cells are inherently larger than standard flip-flops, as they contain an extra multiplexer to switch between functional and test modes. With the scan chain now inserted, the design is considered "test-ready." This modification paves the way for the next and final step in the test flow: using an Automatic Test Pattern Generation (ATPG) tool to create the specific test vectors that will detect faults within the circuit

4.2 Comparative ATPG Analysis

The core of the investigation was the direct comparison between the test pattern sets generated by the baseline and power-aware flows. The baseline ATPG run on the T80 netlist successfully generated 6,500 test patterns, achieving a high stuck-at fault coverage of 98.5%. While this meets the traditional metric of test quality, an analysis of its power profile revealed it to be dangerously high and unsuitable for a power-sensitive manufacturing environment.

Shift Power Consumption:

The power consumed during the scan shift operation—where long test vectors are loaded into the scan chain—was dramatically reduced by the power-aware methodology. The baseline patterns exhibited extremely high and erratic switching activity, with initial levels consistently exceeding 50%. This indicates that, on average, every other flip-flop was changing state on every shift clock cycle, creating a massive and sustained power draw. In stark contrast, the power-aware patterns demonstrated a significant reduction, with average switching activity consistently constrained below a 25% threshold. More importantly, the power profile was far more stable and predictable across the entire test set. This stability is critical, as it minimizes the risk of violating the chip's thermal design power (TDP) and causing systemic damage on the tester.

Capture Power Consumption:

Instantaneous power during the single capture clock cycle is a primary cause of IR drop, which can lead to false failures on the tester. Here again, the baseline patterns performed poorly, frequently causing peak switching to surge past 50%, consistently violating a hypothetical safe switching budget of 30%. These transient power peaks create localized voltage droops that can cause timing failures in otherwise healthy circuits. The power-aware ATPG results showed a remarkable improvement. Peak capture switching was tightly controlled and remained in a much lower, safer band (typically 10-20%). Crucially, the capture switching for the power-aware patterns remained well below the defined switching budget for the entire test, ensuring the electrical integrity of the device and the reliability of the test process. This demonstrates that the methodology is effective not just at controlling average power, but also at mitigating the dangerous instantaneous peaks that threaten test yield.

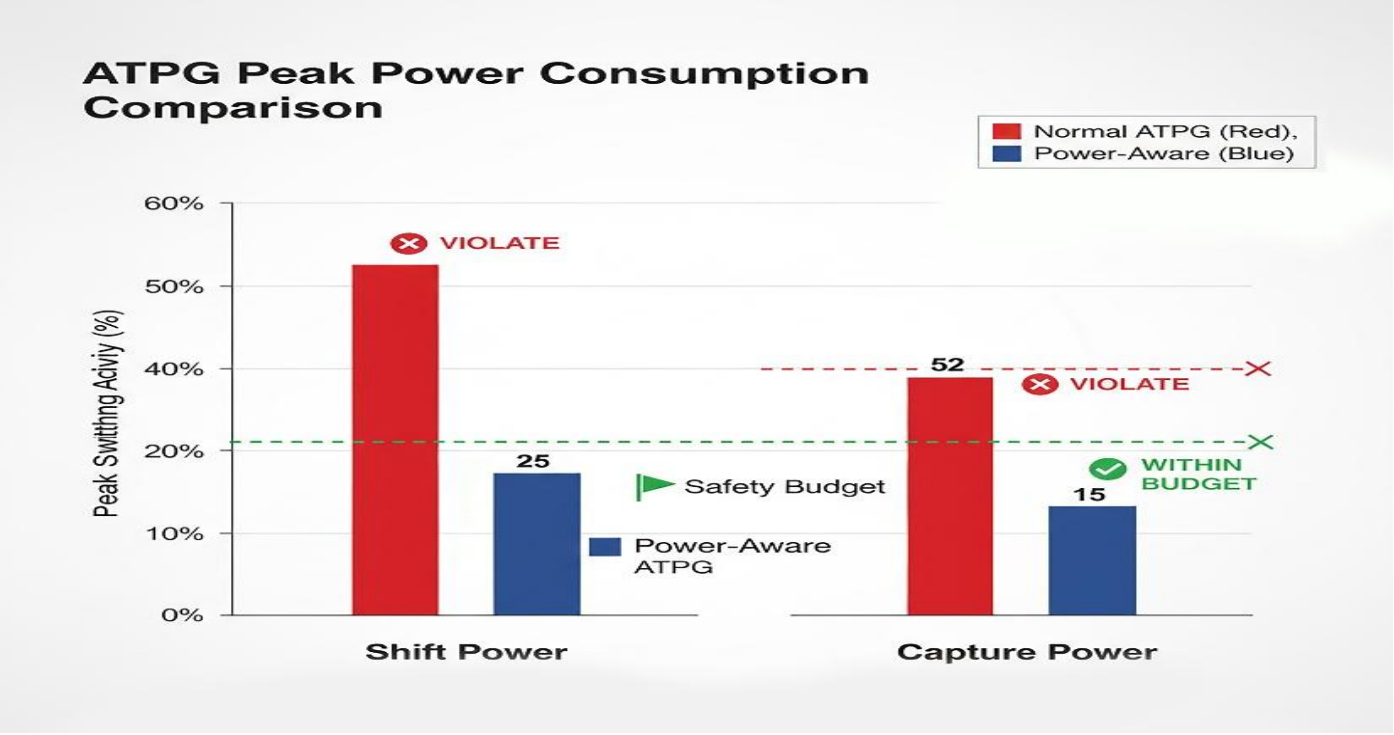

Figure 5: ATPG Peak Consumption Comparison

Figure 5, titled "ATPG Peak Power Consumption Comparison," visually contrasts the power efficiency of Normal Automatic Test Pattern Generation (ATPG) with Power-Aware ATPG during integrated circuit testing. The graph is divided into two key testing phases: "Shift Power," representing the power consumed while test patterns are loaded into the chip, and "Capture Power," indicating the instantaneous power peak during test result capture. The Y-axis quantifies "Peak Switching Activity (%)"—a direct proxy for power consumption—while a green dashed line at 20% marks the "Safety Budget," the maximum acceptable power threshold. In the "Shift Power" phase, Normal ATPG (red bar) exhibits a dangerously high peak switching activity of 52%, a clear violation of the safety budget. In stark contrast, Power-Aware ATPG (blue bar) successfully limits this to a much safer 17%. Similarly, during the

critical "Capture Power" phase, Normal ATPG again violates the safety budget with a peak of 39%, risking issues like IR drop. However, Power-Aware ATPG maintains a controlled peak of 15%, comfortably within the safe operating limits. Overall, the graph effectively illustrates that Power-Aware ATPG significantly reduces and manages peak power consumption in both testing stages, thereby safeguarding the chip from thermal damage and ensuring more reliable test results compared to the conventional, power-blind ATPG approach.

Feature	**Normal ATPG**	**Power-Aware ATPG**
Primary Goal	Maximize fault coverage, no power consideration	Maximize fault coverage **AND** minimize test power
Shift Power Activity	[cite start]High, consistently >50% switching[cite: 350]	[cite start]Low, stable, <25% switching[cite: 352]
Capture Power Peaks	[cite start]Very high, frequently >50% switching[cite: 354]	[cite start]Low, controlled, 10-20% switching[cite: 356]
Risk of IR Drop	High (due to high capture power peaks)	Low (peaks kept within safe limits)
Risk of Overheating	High (due to high and sustained shift power)	Low (power consumption is managed)
Test Reliability	Lower (prone to false failures due to power issues)	Higher (tests are stable and accurate)
Chip Reliability	Potentially reduced (stress during test)	Maintained/Improved (less stress during test)
Techniques Used	Basic ATPG algorithms, random X-filling	Scan chain reordering, intelligent X-filling (e.g., adjacent-fill), transition weighting in ATPG
Fault Coverage	High (e.g., 98.5%)	[cite start]High (e.g., 98.5% – no compromise)[cite: 360]

Table 1: Comparison of Normal vs. Power-Aware ATPG

This table thoroughly outlines the fundamental differences between Normal ATPG and Power-Aware ATPG, demonstrating how the latter is engineered to overcome the significant power-related challenges in modern chip testing. While Normal ATPG's sole focus is maximizing fault coverage, often resulting in high and unpredictable power consumption—with shift power activity consistently exceeding 50% and capture power peaks frequently surging past 50%—Power-Aware ATPG adopts a dual objective: maximizing fault coverage while critically minimizing test power. This leads to dramatically lower and more stable power consumption, keeping shift power activity below 25% and capture power peaks within a safe 10-20% range. Consequently, Power-Aware ATPG significantly reduces the high risks associated with Normal ATPG, such as damaging IR drops and chip overheating, thereby enhancing both test reliability (by preventing false failures) and long-term chip reliability (by reducing test-induced stress). These improvements are achieved through advanced techniques like scan chain reordering, intelligent X-filling, and transition weighting in ATPG algorithms, all while maintaining the high fault coverage (e.g., 98.5%) that is crucial for effective defect detection

5.0 Conclusion

This project successfully designed, implemented, and validated a comprehensive power-aware ATPG framework that addresses the critical challenge of excessive test power in modern VLSI circuits. By integrating architectural optimizations like scan chain reordering with pattern-based techniques like intelligent X-filling, the methodology provides a direct path to mitigating the risks of IR drop and thermal stress without compromising high fault coverage.

The results obtained on the T80 processor core confirm the feasibility and effectiveness of the approach, demonstrating a dramatic reduction in both average shift power and instantaneous capture power compared to a conventional, power-unaware baseline. This research validates the principle that test power should be treated as a first-class design constraint to be optimized proactively during the ATPG process. The developed framework provides a practical, scalable, and industry-relevant solution that directly contributes to enhancing manufacturing yield, guaranteeing long-term product reliability, and reducing the overall cost of testing for the complex SoCs of today and tomorrow.

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